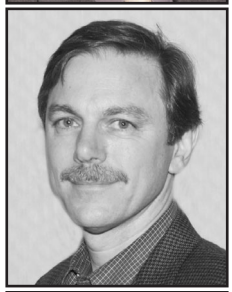
SE6 Highlights of 2005 A-SSCC and Symposium on VLSI Technology



CO-Organizer: Takayasu Sakurai, University of Tokyo, Tokyo, Japan
CO-Organizer: Ian Young, Intel, Hillsboro, OR
CO-Organizer: Takayuki Kawahara, Hitachi, Tokyo, Japan
Chair: Yoshiaki Hagihara, Sony Corporation, Tokyo, Japan

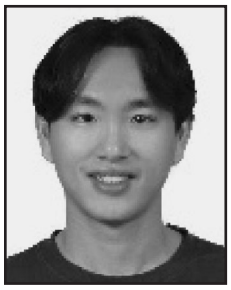
A-SSCC is the international forum for advances in solid-state circuits design held in Asia, and fully supported by the IEEE Solid-State Circuits Society. This conference was newly started in Hsinchu, Taiwan just in 2005. Among the accepting papers through very critical selection meeting, three papers each from Korea, Taiwan, and China, are presented this year. The fields where each paper aims for are widely spread. That represents the totally balanced growth of LSI design in Asia. That are high speed serial link by DLL-based clock edge modulation with 270Mb/s at 3.12mW, 1.2V in 0.18µm, low power analog-digital mix-mode low power IC architecture inside the wireless endoscopic capsule, and differential cascaded-distributed amplifier with pass bandwidth of 100MHz to 25.5GHz in 0.18µm.

On the contrary, Symposium on VLSI Technology has celebrated its twenty-fifth anniversary in 2005, which was held in Kyoto, Japan. This conference has afforded a unique opportunity for engineers and scientists to share the entire VLSI spectrum by paring the Symposium on VLSI Circuits. Since the scope of the symposium includes new concepts and breakthroughs in VLSI devices and processes, three papers related for advanced transistor technology are selected in this year. That are strained-Si directly on insulator to achieve high performance with strict power budgets, 65nm node HfSiON dielectric and body-biasing scheme with Ion of 510/220µA/µm with Istandby of 23/23pA/µm, and 8Å high-performing ultra thin n-channel transistors with TaN-gated HfO2 with a drive-current of 815µA/µm at an off-state current of 0.1µA/µm.

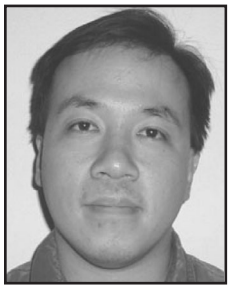
Position Statements

A 3mW 270Mb/s Clock-Edge Modulated Serial Link for Mobile
Won-Jun Choe, Seoul National University, Seoul, Korea
In this paper, a single channel clock-edge modulated serial link for mobile display interface is presented. Clock edge modulation (CEM) enables all necessary signals between a graphics processor and a LCD timing controller to be transferred over a single, DC-balanced differential channel, thus greatly saving the power and costs of the existing parallel lines. A simple DLL-based CEM decoder is described that recovers the data with low power consumption and high jitter tolerance. The use of a voltage-mode driver and a single-side termination further reduces the power. A prototype CEM transceiver was implemented in a 0.18µm CMOS process and dissipates 3.12mW when operating at 270Mb/s and 1.2V.

A Low Power Digital IC Design Inside the Wireless Endoscopy Capsule
Baoyong Chi, Tsinghua University, Beijing, China
This paper proposes an analog-digital mix-mode low power IC architecture inside the wireless endoscopic capsule, which assures that the capsule can implement the diagnoses of whole human digestive tract and provides real time endoscopic image monitoring. A new low complexity and low power digital IC design inside the wireless endoscopic capsule is discussed in detail. To decrease the power consumption, a novel architecture of three-stage clock management is applied for such a system. A new image compression algorithm based on Bayer image format and its corresponding hardware architecture are both presented for low power and low communication data rate application. The digital circuits were verified on FPGAs and have been implemented in 0.18µm CMOS process.



A 0.1-25.5GHz Differential Cascaded-Distributed Amplifier in 0.18µm CMOS Technology
Chihun Lee, National Taiwan University, Taipei, Taiwan
A differential distributed amplifier employs a loss-compensation L section to increase the bandwidth of the interstage by a factor of 3.5. To demonstrate the proposed circuit, a cascaded distributed amplifier with five stages is presented. It has been fabricated in a 0.18µm CMOS process and achieves a gain of better than 15dB and a pass bandwidth of 100MHz to 25.5GHz while consuming 171mW from a 1.9V supply.



Super-Critical Strained-Si Directly On Insulator (SC-SSOI) CMOS Based on High-Performance PD-SOI Technology
Aaron Voon-Yew Thean, Freescale Semiconductor, Austin, TX
Superior isolation with efficient leakage and parasitic capacitance control has enabled partially-depleted (PD) SOI devices to achieve high performance with strict power budgets, demanded by embedded microprocessor applications. Performance-enhanced PD-SOI devices and circuits based on SC-SSOI technology were demonstrated recently. This presentation describes the performance of SC-SSOI CMOS realized through advanced wafer-bonding technology and Freescale's HiPerMOS-SOI process. The advantages of super-critically thick SSOI over ultra-thin SSOI and bulk strained-Si/SiGe devices will be discussed. Furthermore, the issues of SSOI strain stability and the influence of process-induced stresses will also be described. The presentation will focus on the behavior of aggressively scaled transistor under high biaxial strain and highlights its impact on transistor electrostatics, gate leakage and electronic transport. In addition, some of the scaling issues relating to parasitic resistance and velocity saturation in the context of channel strain engineering will be identified as well.

Ultra-Low Standby Power (U-LSTP) 65nm node CMOS Technology Utilizing HfSiON Dielectric and Body-biasing Scheme
Naohiko Kimizuka, NEC Electronics, Kanagawa, Japan
This paper reports 65nm node ultra-low standby power CMOS technology, utilizing reverse body-biasing and Vdd control scheme. Standby leakage (Istandby) corresponds to sum of gate leakage (Ig), gate induced drain leakage (IGIDL) and subthreshold leakage (Isubth). By using nitrided hafnium silicate (HfSiON) film as gate dielectric, we have reduced Ig. With well-optimized fabrication process, we could improve Ion, simultaneously. The record Ion/Istandby ratio, Ion of 510/220µA/µm with Istandby of 23/23pA/µm, are obtained at Lg=55nm. Improvement of circuit performance will be presented. We have also confirmed reverse body-biasing scheme feasibility for further Ioff reduction. By exploiting gate-electrode work-function modulation due to HfSiON layer formation, we have reduced the channel impurity concentration and suppressed IGIDL even under reverse body-biasing condition. Istandby was reduced to 1.4pA/µm for nFET and 0.32pA/µm for pFET at Vdd= 0.8V and Vb= ±1V, which is the smallest value ever reported for 65nm node LSTP. We have also investigated reduction of Vth fluctuation by channel engineering and reverse body-biasing.

High Performing 8Å EOT HfO2 / TaN Low Thermal-Budget n-channel FETs with Solid-Phase Epitaxially Regrown (SPER) Junctions
Lars-Åke Ragnarsson, IMEC, Leuven, Belgium
We demonstrate high-performing ultrathin n-channel transistors with TaN-gated HfO2. A low temperature (570°C) process with solid-phase epitaxially regrown (SPER) junctions was used to avoid interfacial oxide regrowth, achieve low EOT and scalable high-performing devices. The thinnest devices have an EOT of 8.3Å, a leakage current of 2.6 A/cm^2 at VG=1V, and a drive-current of 815µA/µm at an off-state current of 0.1µA/µm for VDD=1.2V. Improvements in channel electron mobility were achieved by decreasing the thickness of the HfO2 resulting in less charge-trapping in the dielectric and hence less Coulomb scattering. The drive-current improvement over identical gate-stacks processed with a 1000°C spike anneal is 20-25% and is related to the lower VT achieved as a result of the low thermal budget.